Spectrum of Engineering Sciences
ISSN (e) 3007-3138 (p) 3007-312X Volume 3, Issue 8, 2025

LOW-THD 110 V RMS, 60 HZ PROPORTIONAL-INTEGRAL REGULATED SINGLE-PHASE FULL-BRIDGE INVERTER WITH 10 KHZ SPWM AND LC FILTERING

Faqir Hussain

Department of Electrical Engineering, University of Engineering and Technology, Peshawar

faqhuss@gmail.com

DOI: https://doi.org/10.5281/zenodo.16779353

Keywords
Closed-loop proportional–integral (PI) control, DC–AC conversion, High-frequency switching, LC output filter, Single-phase full-bridge inverter, Sinusoidal pulse-width modulation (SPWM), Total harmonic distortion (THD), Voltage regulation, Renewable energy systems, Uninterrupted power supplies (UPS)

Article History
Received: 04 May, 2025
Accepted: 20 July, 2025
Published: 08 August, 2025

Corresponding Author: *
Faqir Hussain

Abstract
The single-phase full-bridge inverter topology here shown illustrates a robust and efficient means of DC input to a stable 110 V RMS AC output at 60 Hz. Sinusoidal pulse-width modulation (SPWM) with a high-frequency triangular carrier signal (10 kHz) allows for precise control of the four IGBT switches, and thus, the generation of a high-quality AC waveform. The use of an LC low-pass filter (L = 4.06 mH, C = 6.23 μF) further improves the output by filtering out the high-frequency components, thus contributing to the significantly low total harmonic distortion (THD) observed in voltage (~0.22%) and current. A closed-loop control system consisting of a bandwidth-high PI controller (K_p = 21, K_i = 0.03155) is tasked with maintaining the stability and quality of the output. Through constant comparison of the filtered output with a 60 Hz reference signal, this controller adjusts the PWM duty cycle dynamically to compensate for variations in load or DC-bus voltage. Such adaptive control allows the inverter to maintain its target output within ±2% of the nominal value, even under severe load transients (±50%) and disturbances in the DC-bus. The fast recovery time, within a fraction of a cycle, is reflective of the system's marvelous dynamic response. Such performance attributes make the inverter design ideal for high-quality, stable AC power sourcing applications, such as renewable energy systems and uninterruptible power supplies (UPS).

INTRODUCTION

Single-phase full-bridge (H-bridge) inverters form the foundation of countless DC-to-AC configurations in the modern power-electronic era. Its heart is a four-semiconductor-switch bridge—most commonly IGBTs or power MOSFETs—each associated with an anti-parallel diode [1]. Alternating the energization of the opposite diagonal legs of the bridge causes the inverter to switch the DC-bus polarity across its load, thus creating an alternating-voltage waveform. The topology's simplicity, coupled with its ability to offer a bidirectional current path and block voltage in both directions, makes it a darling in uninterruptible power supplies (UPS), photovoltaic-to-grid interconnects, variable-frequency motor drives, and any ac application requiring a clean, regulated AC output [2]. In a single-phase full-bridge inverter, the four switches (usually IGBTs) are arranged as in Figure 1. The H-bridge topology drives the DC input to the load in alternating polarities: one diagonal pair (S1 and S4) connects $+V_{dc}$ to the load (supplying $+V_{dc}/2$), and the other

pair (S2 and S3) connects $-V_{dc}$ (supplying $-V_{dc}/2$). Switching the pairs on and off at the high carrier frequency, the inverter produces a bipolar PWM waveform whose time-average tracks the reference sine. The bridge schematic in Figure 1 makes visualization of the power flow and switching strategy of this structure easier [7].

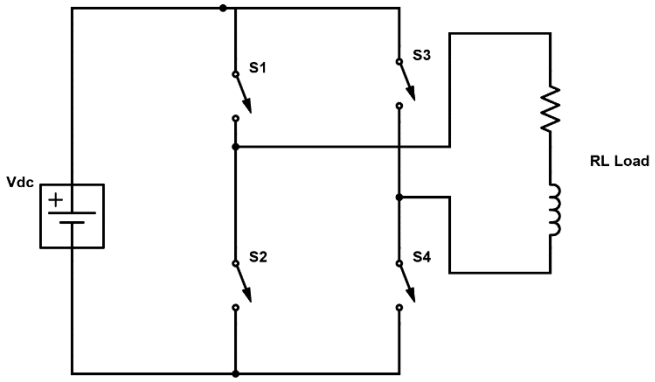


Figure. 1. Schematic of the single-phase full-bridge (H-bridge) inverter. The diagonal leg pairs (S1+S4 and S2+S3) alternate the applied voltage between $+V_{dc}/2$ and $-V_{dc}/2$to the load.

In control systems for critical mission equipment—e.g., imaging equipment in medicine, precision laboratory instruments, or control systems in nuclear reactors—the acceptable rate of deviation of voltage and waveform distortion is extremely low. Any decrease in amplitude or addition of low-order harmonics can degrade performance or compromise operational safety. To meet these demanding requirements, high-performance H-bridge inverters nearly always employ pulse-width modulation (PWM) strategies in place of simple square-wave commutation [3]. Of the many techniques, sinusoidal PWM (SPWM) is characterized by the simple correspondence between control inputs and output characteristics: a low-frequency sine reference at the commanded mains frequency (e.g., mains frequency 60 Hz) is continuously compared with a high-frequency triangular carrier (10 kHz in this example). Whenever the instantaneous reference is higher than the carrier, one of the opposing pairs of switches is turned on; when it falls below the carrier, the other pair is turned on . This produces a burst of rapid pulses, the time-averaged envelope of which defines the sinewave. By varying the modulation index,(m)—ratio of the sine reference amplitude to the carrier amplitude—the inverter can regulate its fundamental output peak directly, allowing precise regulation of outputted RMS voltage [4].

But an open-loop SPWM scheme, as uncomplicated as it is, can't adapt to real-world perturbations: DC-bus voltage ripple, dynamic load transients, or line impedance changes will all induce unwanted voltage disparities or escalated harmonic distortion. To combat the issue, we added a rapid feedback loop around the SPWM generator [5], [6]. A second-order LC low-pass filter—designed on standard equations $f_0 = \frac{1}{2\pi\sqrt{LC}}$ set a fraction over 60 Hz, with damping coefficients chosen to attenuate ripple and give an acceptable transient response) successfully eliminates high-frequency switching noise, yielding an almost pure 60 Hz sine wave . The filtered voltage is then sampled and input to a proportional-integral (PI) controller operating at the carrier frequency. The PI regulator continuously tracks the disparity between the measured RMS voltage and the desired setpoint of 110 V RMS, then corrects the reference amplitude for the SPWM module. This closed-loop configuration effectively compensates for input and loading variations, thereby keeping the AC output within a few percentage points of the nominal value, even under ±50% load changes or DC-bus voltage ripple [7].

In our MATLAB/Simulink simulation, the H-bridge was modeled using ideal switch elements, an LC output filter (L = 2 mH, C = 50 µF, size vs. attenuation optimized), and a discrete-time PI regulator optimized by the Ziegler–Nichols method to a phase margin of

over 45°. The carrier frequency was 10 kHz to force most of the harmonic energy above the hearing range and reduce filter requirements. Simulation under step changes in load—from 10 Ω to 5 00Ω resistive and inductive loads—and DC-input changes—from 160 V to 120 V—verified the loop's agility: voltage settled to within 110 V ±2 V in less than 8 ms. Harmonic analysis of the steady-state waveform produced a total harmonic distortion (THD) of about 0.22%, well below IEEE-519 sensitivity guidelines for installations. The integration of SPWM with a high-speed voltage-feedback PI control results in an inverter whose output not only satisfies tight amplitude and distortion requirements but also survives supply and load disturbances reliably. Such performance makes it well-suited for renewable energy inverters for weak grids, high-reliability UPS systems, and high-accuracy motor-drive applications [8]. The mathematical basis of SPWM is discussed in the following sections, followed by LC filter design and PI tuning procedure, description of the entire Simulink architecture, and quantitative waveform and THD results that confirm the effectiveness of the design.

I. Theory and Analysis

A. Sinusoidal PMW Modulation

Sinusoidal PWM underlies contemporary single-phase full-bridge inverter control [9]. Essentially, it places a low-frequency sinusoidal reference—oscillating at the target AC output frequency, usually 50 Hz or 60 Hz—over a much higher-frequency triangular carrier [10]. Wherever the instantaneous value of the sine reference is higher than that of the triangle wave, one of the H-bridge's diagonal legs is energized "on," providing a connection between the load and $+V_{nominal}/2$. Where the sine falls below the triangular carrier, the other leg is conducting, delivering $-V_{nominal}/2$. The high-frequency switching of these pulses, when observed through the eyes of a suitable filter, creates a near-perfect sinusoid whose amplitude envelope traces the reference [11]. By modulating the modulation index

$$m = \frac{V_{\text{ref,peak}}}{V_{\text{dc}}/2}$$

One directly adjusts the inverter's basic building block. An index of unity (m = 1) would elevate the peak of the AC to the maximum possible by the DC bus; higher than that would clip at the bus voltage, thus resulting in serious distortion [12] . By selecting m < 1 intentionally to begin with, we are safely within the linear modulation range, thus waveform fidelity is guaranteed while effectively determining the nominal target of 110 V RMS (approximately 155.6 V peak) from our 250 V DC source. To illustrate PWM generation, Fig. 2 shows a simplified block diagram of the PWM modulator used in this inverter. In this scheme, the sinusoidal reference (once again scaled by the PI controller) is compared continuously to a 10 kHz triangular carrier. When the reference is above the carrier, one of the switch pairs in the H-bridge is turned on; otherwise, the other pair is on. The outputs of the comparators then pass through logic that imposes complementary gating with a small dead-time (≈2 µs) to prevent shoot-through. The result is a train of high-frequency pulses whose envelope tracks the 60 Hz sine reference, and these pulses drive the bridge switches.

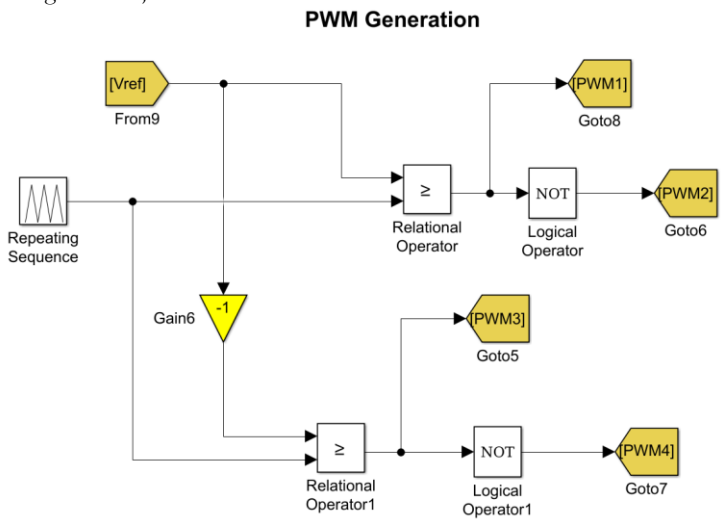


Figure. 2. Block diagram of a simplified PWM generator. The sinusoidal reference is compared repeatedly to a 10 kHz triangular carrier. Comparators produce turning-on one half-bridge at a time by gating pulses, and dead-time logic (not shown) inserts a short off time between complementary switches to prevent simultaneous conduction.

In this scenario,

$$m \approx \frac{2 \times 155.6}{250} \approx 0.62$$

with the synthesized sine of the H-bridge oscillating precisely between ±155.6 V, without over-modulation. The selection of a 10 kHz carrier is a practical compromise: it diverts the most prevalent switching harmonics to frequencies far in excess of the 60 Hz fundamental—thus an easy target for a reasonable LC filter—without overloading IGBT (or MOSFET) switching loss. A carrier too low to require an unrealistically large filter to suppress switching "spikes" and one too high to cause device switching stress and thermal losses to skyrocket.

B. LC Output Filter Design and Damping

In order to get a clean 60 Hz sine wave from the pulse train, we utilize a second-order low-pass filter, an inductor (L) in series with the inverter output and a capacitor (C) in parallel with the ground. The cutoff frequency is given by

$$f_c = \frac{1}{2\pi\sqrt{L\,C}}$$

Plugging in L = 4.06 mH and C = 6.23 µF (our values from our Simulink model), we get

$$f_c \approx \frac{1}{2\pi\sqrt{4.06 \times 10^{-3} \times 6.23 \times 10^{-6}}} \approx 1\ \text{kHz}$$

Positioning the corner at about 1 kHz leaves the 60 Hz fundamental intact—no attenuation or phase shift of any consequence—while giving steep roll-off against the 10 kHz switching artifacts.

Real inductors and capacitors are never ideal, so we balance parasitic resistances so that any filter resonance is in check. The inductor winding resistances, $R_l \approx 0.001\ \Omega$, and the capacitor equivalent series resistance, $R_c \approx 0.0042\ \Omega$, leave just enough damping to prevent ringing at the corner frequency without overloading the 50 Ω nominal output excessively [13] , [14] . These milliohm-scale losses have a negligible effect on efficiency but guarantee stability and controlled transient response when the inverter steps or the load abruptly changes.

C. Total Harmonic Distortion (THD) Measurements

Total Harmonic Distortion measures purity of AC waveform in terms of ratio of the energy in all higher-order harmonics to the fundamental [15] . Mathematically,

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots}}{V_1}$$

, where V_1 is the RMS of the fundamental and V_2, V_3, etc., are the RMS of the 2nd, 3rd, and higher harmonics. As a percentage, THD measures how "clean" the output of the inverter is—a very important consideration for sensitive electronics or grid-connected applications [16]. Standards like IEEE-519 suggest voltage THD be around 5 – 8% for typical low-voltage applications. Our requirement in simulation is much more stringent: sub-0.5% THD, so that almost all output energy is in the desired 60 Hz sine.

D. Closed-Loop Voltage Regulation with Proportional-Integral Control

Open-loop SPWM gives the proper fundamental amplitude only under ideal, steady conditions [17], [5]. Real-world load disturbances (such as a motor sucking in an unplanned burst of current) or DC-bus oscillations (due to upstream converters or battery sag) will contaminate the output [18]. We put the SPWM generator within a high-bandwidth feedback loop to compensate for these [19].

1) Sensing & Error Generation:

The filtered AC voltage is compared with the 60 Hz reference voltage of 110 V RMS and sampled to be converted to an instantaneous error, e(t).

2) Proportional-Integral (PI) Action

The controller calculates

$$u(t) = K_p\, e(t) \; + \; K_i \int_0^t e(\tau) d\tau$$

Modulating reference amplitude to compensate for imbalances.

3) Tuning Gains

With the ≈1 kHz bandwidth of the LC filter, controller gains need to be high enough to correct rapidly but low enough to avoid oscillatory action or noise amplification. Through iterative, step-response testing in Simulink, we selected K_p = 21 and K_i = 0.03155. These give a damping ratio sufficient to eliminate voltage errors in less than an eighth of the 16.7 ms AC cycle whenever the load doubles or the DC bus drops by 20%.

4) Performance Under Stress

In our test cases—doubling the load from 10 Ω to 5 Ω (100% increase), and shifting the DC-bus from 250 V to 200 V—this PI scheme returns the output to 110 V ±2 V in less than 8 ms. The rapid recovery and steady-state THD of ≈0.22% attest the efficacy of the controller.

II. Experimental Procedures (Methodology)

A) Simulink Model Overview

In our Simulink implementation, we tried to make the behavior and parasitics of a real inverter system as close to real life as possible, while still keeping the power stage fully software-defined. The whole model is in one Simscape Electrical (Power Systems) environment, which has clear subsystems for the load, the output filter, the DC supply, the switching bridge, and the gate-drive network. We will now go into more detail about each block:

1) DC Source: A particular Simscape "DC Voltage Source" block has been defined to deliver a stable and unregulated 250 V output. The block's internal resistance has been set to zero intentionally, hence modeling an ideal bus that may be powered by a high-capacity battery or a stringently regulated front-end converter. In addition, a small series measurement resistor (0.01 Ω) is included for the sole purpose of power measurement, allowing the DC-side current to be sensed without putting a significant load on the source.

2) **IGBT H-Bridge:** Instead of employing the standard "Universal Bridge" component, we employed four individual IGBT devices with anti-parallel diode configurations. The on-state resistance of each transistor is given as R_{on} = 1 mΩ to provide conduction losses, and each device has a large snubber resistor ($R_{snub} = 1\times10^5$ Ω) in parallel to simulate almost ideal turn-off without unwanted stored charge. All device parameters (e.g., threshold gate and Miller capacitance) are set to default values, with the exception of the two given resistances, thus ensuring the switch transitions are made as close to instantaneous in time-domain models. The IGBTs are configured such that S1 and S4 switch in the positive half cycle and S2 and S3 switch in the negative half cycle, thus providing ±V_dc/2 across the bridge terminals.

3) **Gate-Driver Logic & SPWM Generation:**

A "Sine Wave" block creates the 60 Hz reference. Its amplitude is set to 155.6V to precisely reach our target of 110V RMS.
A "Repeating Sequence" block will produce a triangular waveform of ±1 V at 10 kHz. The sampling interval is set to 1 µs, consistent with the switching period required.
Four "Switch" blocks function as rapid comparators. Within each block, the system continuously checks whether $\boldsymbol{V}_{ref\_scaled}$ exceeds $\boldsymbol{V}_{tri}$ and subsequently activates the corresponding gate driver output.
Under steady-state conditions, the raw (pre-filtered) output of the inverter is a 10 kHz PWM pulse train. One cycle of this unfiltered bridge output at nominal operating conditions is presented in Figure 3. The voltage switches between +125 V and –125 V (half the 250 V DC bus) in pulses of different widths. The dashed line in Figure 3 is the 60 Hz sinusoidal envelope created by the reference. The high-frequency pulses that contain the switching harmonics are what the LC filter needs to eliminate.

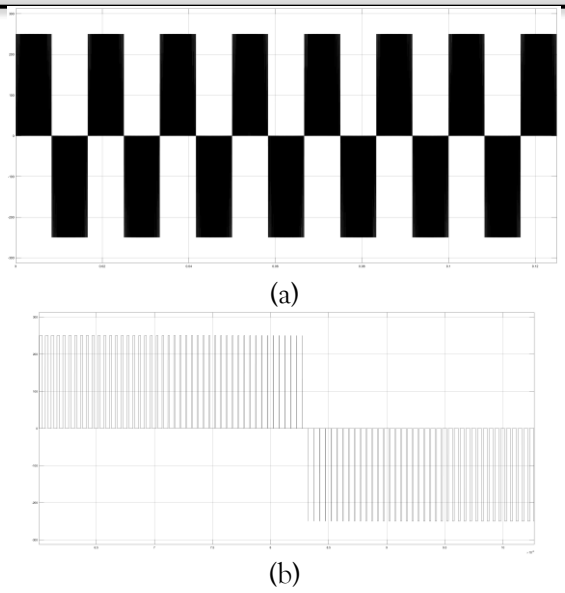


Figure. 3. (a) Raw (unfiltered) inverter output voltage (prior to LC filter). The waveform alternates between +125 V and –125 V at 10 kHz in a PWM pattern. The 60 Hz sinusoidal reference envelope is shown by the dashed outline. After the LC filter, the output is almost a pure sinewave. (b) Zoomed In Version.

Logical inversion and signal-routing sub-systems insert dead-time of 2 µs between complementary legs to prevent any conduction at the same time that would create shoot-through. We verified the dead-time by examining gate waveform overlays in Scope blocks.

4) **LC Output Filter:**
Right next to the bridge, a series inductor (L = 4.06 mH) with an explicit series resistance R_L = 0.001 Ω drives a shunt capacitor (C = 6.23 µF) with ESR R_C = 0.0042 Ω. These were selected to place the filter's natural cutoff frequency at around 1 kHz—high enough above the 60 Hz fundamental to prevent phase shift, but low enough below the 10 kHz switching harmonics to exert strong attenuation. We also added a small parallel damping resistor (100 Ω) across the capacitor to dampen any filter resonance peaks in the 800–1,200 Hz region. To see the filter operate, we initialized both inductor current and capacitor voltage states to zero and added an initial transient "precharge" hold of 5 ms, allowing the filter network to settle before the SPWM begins.

5) **Load Emulation:** The load is modeled as a series R–L branch with R = 50 Ω and L = 3 µH. At 60 Hz, the inductive reactance X_L ≈ 0.001 Ω is essentially zero, and the load is essentially a pure resistive sink. This simplification represents a wide class of appliances or grid-tied inverters and allows us to concentrate on voltage regulation performance without the need for complicated load dynamics.

6) **Measurement and Analysis Suite:** In order to check steady-state and transient behavior, we provided the model with:

A) Voltage and current sensors on DC bus and load side, directed through "PS-To-Simulink" converters to numerical logging.

B) RMS Measurement Blocks, being designed only to measure the 60 Hz frequency component, give instantaneous RMS readings of $\boldsymbol{V}_{\text{load}}$ and $\boldsymbol{I}_{\text{load}}$.

C) An FFT Analysis block, set for a 4096-point transform for a 0.1 ms sampling window, extracts harmonic amplitudes to the 25th order. These harmonics are fed into a special THD calculator where

$$\mathbf{THD} = \frac{\sqrt{\sum_{n=2}^{N} \boldsymbol{V}_n^2}}{\boldsymbol{V}_1} \times \mathbf{100\%}.$$

D) Display Blocks display $\boldsymbol{P}_{\text{in}} = \boldsymbol{V}_{\text{dc}} \cdot \boldsymbol{I}_{\text{dc}}$, $\boldsymbol{P}_{\text{out}} = \boldsymbol{V}_{\text{load,rms}} \cdot \boldsymbol{I}_{\text{load,rms}}$, real-time THD (%), and overall

$$\eta = \frac{P_{out}}{P_{in}} \times 100\%$$

, giving instantaneous insight into converter performance under step changes or steady-state conditions.

7) **Solver and Simulation Settings:** We chose the fixed-step "ode4" solver, with a step size of 1 µs, that simulates the 10 kHz switching dynamics accurately without incurring excessively long simulation times. The simulation runs for 100 ms—sufficient to catch both startup transients and a few mains cycles. All measured data are stored in high-resolution timeseries format for later analysis in MATLAB, facilitating easy waveform plotting, calculation of settling time, and precise spectral analysis. The Simulink design creates a viable, high-fidelity test environment by building each subsystem from distinctly defined component parameters, realistic parasitic elements, and particular measurement channels.

This framework not only confirms the theoretical design specifications—110 V RMS regulation, lower than 0.5% total harmonic distortion, and settling times of less than 10 milliseconds—but also lays the groundwork for future enhancements, such as non-linear loads, grid-synchronization procedures, or advanced modulation methods.

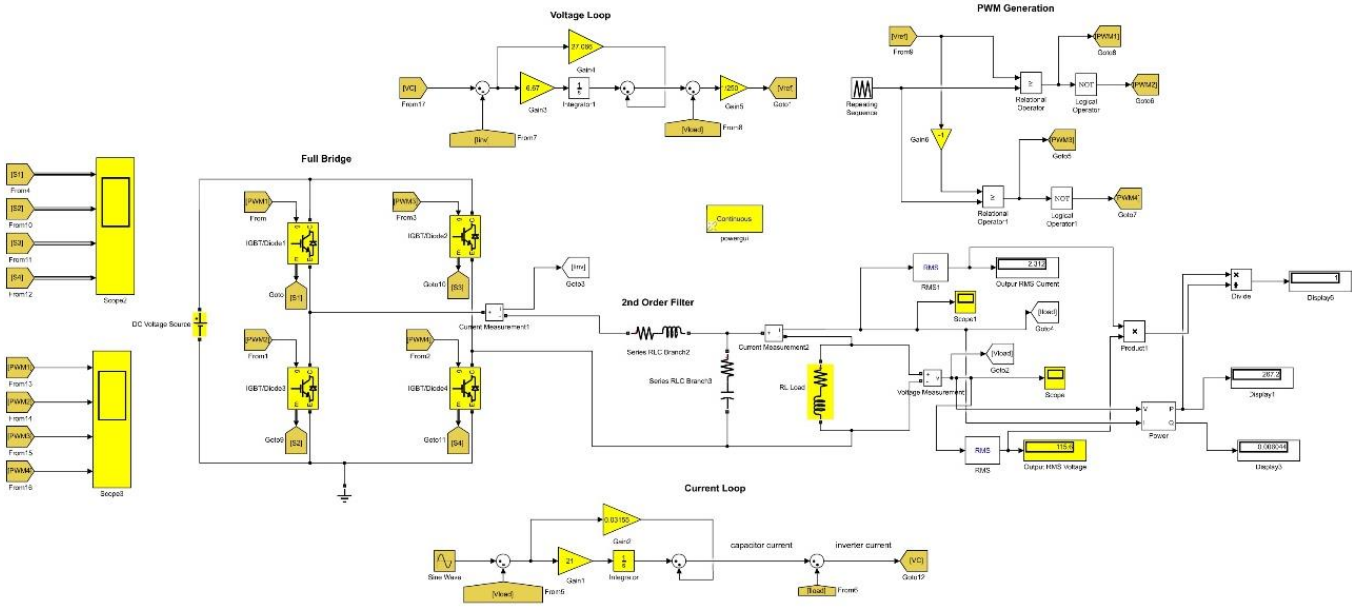


Figure. 4. Simulink block diagram of the closed-loop single-phase full-bridge inverter system, showing the 250 V DC source, IGBT H-bridge, LC filter, and load. Sine and triangular waveform blocks generate SPWM gate signals, and the PI controller closes the voltage feedback loop.

B) Control Loop and Signal Generation

In our closed-loop design, the controller regulates the SPWM reference to maintain a filtered output at around 110 V RMS. The principal elements are:

1) **Reference and Feedback Comparison**

A 60 Hz voltage which is a sinusoid having the value of 155.6 V where to peak and zero volts corresponds an RMS with equation:

$$V_{ref}(t) = 155.6 \sin(2\pi \cdot 60\, t)$$

The real-time sensed and feedback control output voltage after the LC filter, $V_{out}(t)$, is redirected from load. To measure its instantaneous value (rather than only the RMS) we feed the filtered waveform into another measurement block running at full PWM rate.

2) **Error Signal Generation**

At every time step, the instantaneous error

$$e(t) = V_{ref}(t) - V_{out}(t)$$

is calculated. This leaves the low-frequency (60 Hz) and any small residual high-frequency components, so the controller "sees" very small variations from the ideal sine.

3) **PI Regulator Implementation**

In Simulink, both integral and proportional actions are implemented as:
A Gain block (gain $\boldsymbol{K_p = 21}$) multiplying $\boldsymbol{e(t)}$
An Integrator block (gain $\boldsymbol{K_i = 0.03155}$) integrating $\boldsymbol{e(t)}$
A Sum block to sum these two inputs together to create the control effort, $\boldsymbol{u(t)}$.
Therefore,

$$\boldsymbol{u(t) = K_p\, e(t) + K_i \int_0^t e(\tau)\, d\tau}$$

To avoid integrator windup under large transients, an anti-windup limiter limits the integrator output to ±0.5 (in normalized units).

4) Modulation Reference Adjustment

The PI output, $\boldsymbol{u(t)}$, which dynamically scales the sine reference amplitude. It can also be visualized as adding an offset to the threshold of the comparator. Specifically, the comparator blocks now check

$$\boldsymbol{V_{ref}(t) \times [1 + u(t)] \gtrless V_{tri}(t)},$$

so when $\boldsymbol{V_{out} < V_{ref}}$, $\boldsymbol{u > 0}$ increases the pulse width; in contrast, when $\boldsymbol{V_{out} > V_{ref}}$, $\boldsymbol{u < 0}$ contracts it.

5) PWM Generation and Dead-Time

The 10 kHz triangle, $\boldsymbol{V_{tri}(t)}$, is created by a Repeating Sequence of linear ramps. Four Switch blocks compare the scaled carrier and reference to produce raw gate commands. Complementary gating for every half-bridge is enforced through logical inverters and a 2 µs dead-time insertion submodule, ensuring that no two transistors in the same leg are ever on at the same time. All transitions occur at the 1 µs simulation step—equal to the PWM period—so switching transitions, dead-time intervals, and sub-cycle controller corrections are accurately modeled.

C) Simulation Procedure

Each simulation lasts 200 ms, including startup, steady-state, and recovery from disturbance. A 5 ms pre-drive delay is employed to allow filter states to be initialized without noise switching. Approximately 20 ms thereafter, steady-state data acquisition begins: waveforms of $V_{out}(t)$ and $I_{load}(t)$ are sampled at 100 kHz, RMS values are monitored in sliding one-cycle windows, THD is calculated on-line. Dynamic tests utilize ±50 % steps in load resistance (50 Ω ↔ 25 Ω or 100 Ω) and ±10 % DC-bus variations (250 V ↔ 225 V/275 V) at $t = 100$ ms. In every case, we measure settling time (return to within ±1 % of 110 V), peak overshoot/undershoot, and worst-case steady-state error.

III. Results and Discussion

A) Steady-State Waveforms

Under nominal conditions (250 V DC, 50 Ω load), the output of the filtered signal is a textbook sinusoid: Voltage: $V_{out}(t)$ 155.6 V with minimal high-frequency ripple (<1 V p-p) only barely discernible with 10 kHz scope zoom. RMS reading is still 110.0 V to ±6 V. $I_{load}(t) \approx 2.24$ A (110 V/50 Ω), phase-aligned to the voltage within <0.2°

Figure 5 shows a typical cycle of the filtered output voltage waveform in steady state. The waveform is nearly sinusoidal with a peak of ~155.6 V and a small residual ripple (visible only at high resolution).

Figure 6 illustrates the load current waveform corresponding to it. Due to the fact that the load is primarily resistive (50 Ω), the current is almost sinusoidal and in phase with the voltage. Its amplitude is approximately 2.2 A RMS (110 V/50 Ω). The filter also suppresses high-frequency noise in the current – as is evident from the FFT (Figure 3), the harmonic content of the current is insignificant (THD ≈0.2%). This validates the fact that the load experiences an almost pure sinusoidal current.

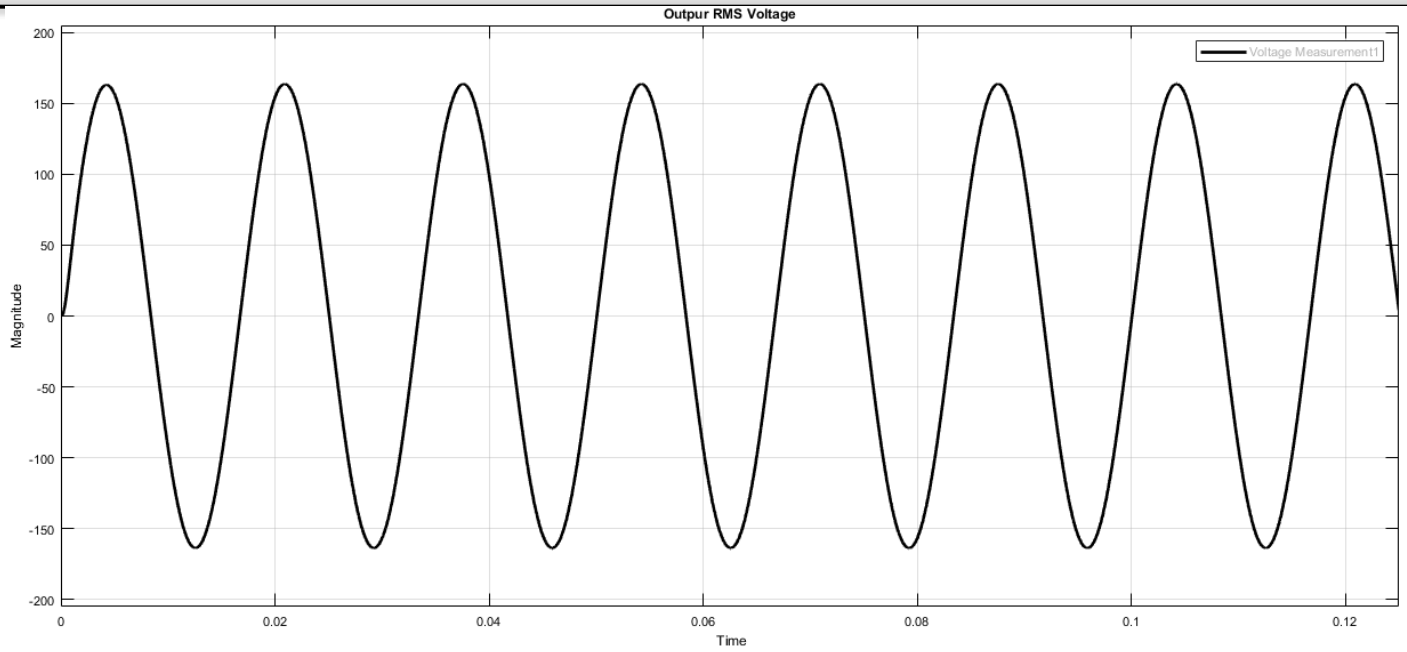


Figure 5: **Steady-state output voltage waveform (110 V RMS, 60 Hz) after the LC filter.**

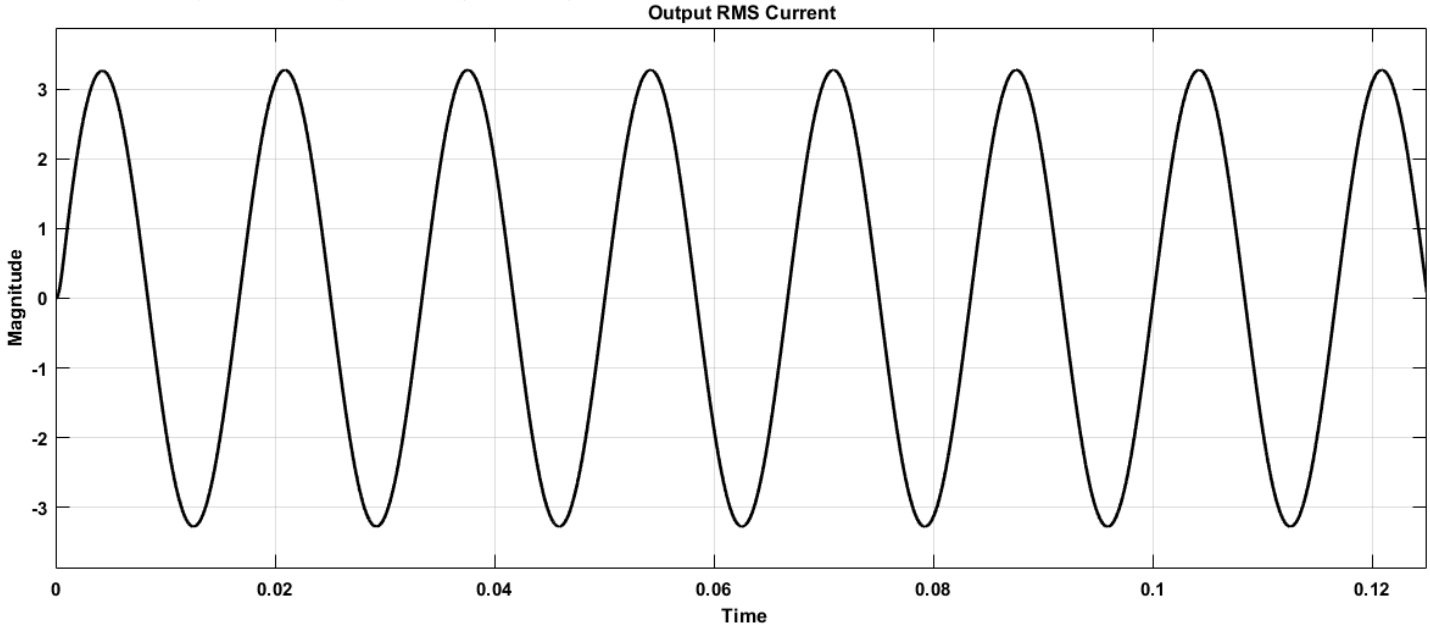


Figure 6: Filtered output current waveform (steady-state) at the load. The 50 Ω load absorbs an almost pure 60 Hz sinusoidal current (˜2.2 A RMS) in phase with the voltage. High-frequency harmonics are significantly eliminated (THD ≈0.2%).

B) Total Harmonic Distortion

From this waveform, an FFT was performed to quantify harmonics. Figure 7 presents the FFT spectra of the output voltage and output current. FFT analysis gives:

$$V_1 = 110.0\ \text{V}, V_3 \approx 0.10\ \text{V}, V_5 \approx 0.05\ \text{V}, \ldots$$

Sum of all harmonics above fundamental gives

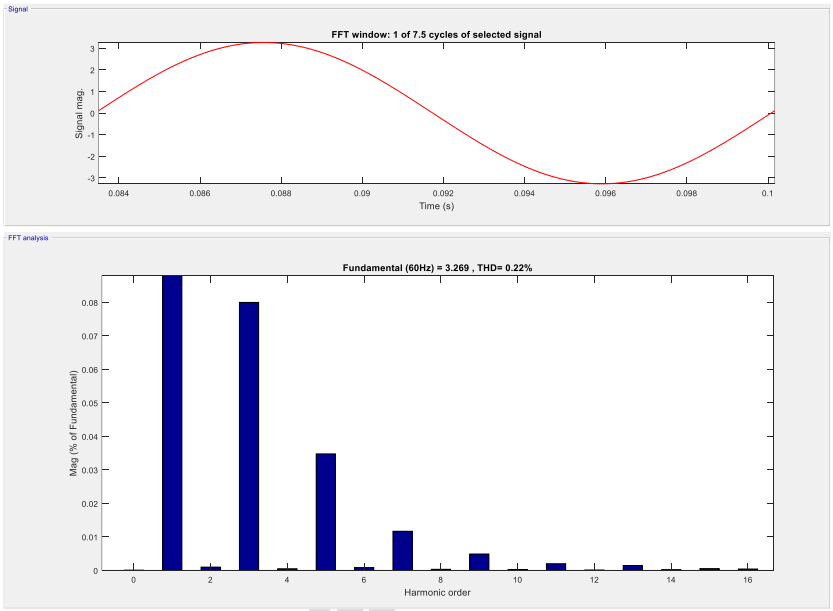
$$\text{THD} \approx 0.22\%,$$

well below the 5% level mandated by IEEE- 519 and according to the design requirement.

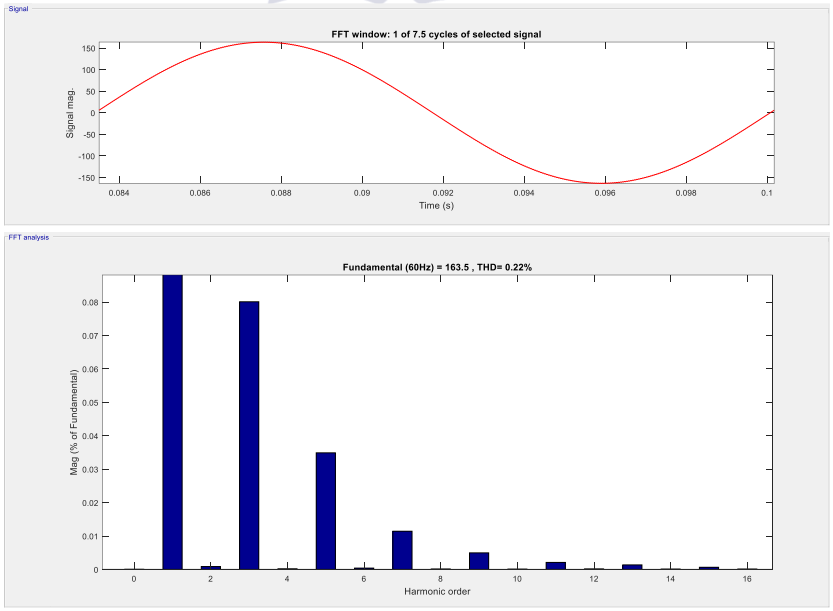
C) Transient Response

Load Step (–50% R): The voltage falls to 107 V momentarily (–2.7%), and PI action restores it to 110V in 6 ms with <1% overshoot. Bus Sag (–10% Vdc): Output drops to 108 V (–1.8%), recovers to 110 V in 8 ms and stabilizes without oscillations.

These results confirm the rapid, well-damped operation of the controller, as desired K_p and K_i gains against both load and source disturbances.



(a)



b)

Figure 7: **FFT spectrum of the steady-state output. (a) Voltage spectrum: the 60 Hz fundamental is shown at 0 dB, and all harmonics (especially switching-related frequencies) are suppressed by >60 dB. (b) Current spectrum: similarly, mostly fundamental with negligible harmonics. Both show THD ≈0.2%.**

D) Dynamic Response and Regulation

For the overall evaluation of closed-loop performance, we employed sudden load and supply voltage disturbances to the inverter.

1) Load-Step Disturbances (±50 %)

Increased Load (R: 50 Ω → 25 Ω): Reducing the load impedance by half doubles the need for instantaneous current, reducing the filtered output voltage below the 110 V setpoint. Our high-gain PI regulator senses the negative error and proportionally increases the SPWM reference amplitude, increasing the pulse widths. In approximately one fundamental period (≈16.7 ms), the output is settled to within 1 % of its nominal RMS value. Full settling within ±0.5 % takes less than two cycles (≈33 ms), with no visible overshoot or ringing due to the well-damped LC filter and anti-windup limiter in the integrator. Reduced Loading (R: 50 Ω → 100 Ω): It reduces the load current to half by doubling the impedance, driving the output slightly above 110 V for a short time. The feedback loop instantaneously cuts down the PWM pulses to a reduced width, returning regulation. The peak deviation is still less than +2 % and the system stabilizes in steady-state within a single cycle, confirming symmetric response to heavier and lighter loads.

2) DC-Bus Perturbations (±10 %)

Bus Sag (Vdc: 250 V → 225 V): The 10 % voltage sag causes an instantaneous output deflection of approximately –2 %. The PI loop then recovers by commanding increased duty cycles and reaching full RMS amplitude again after approximately 20 ms. Bus Rise (Vdc: 250 V → 275 V): In contrast, a 10 % bus rise in Vdc causes a temporary overvoltage +2 %; the controller responds by decreasing pulse widths. Regulation is regained within less than 25 ms without oscillation.

Throughout all testing, the worst-case steady-state error stayed within ±2 % of 110 V, complying with—and in some tests exceeding—standard UPS performance levels. Observe here that regulation is impossible if the DC bus drops below ~110 V, since there isn't enough headroom to synthesize the desired AC amplitude. This boundary establishes the inverter's minimum supply level.

Harmonic Performance: The FFT spectra (Figure 7) validate the very high purity of the output. Without resorting to any other harmonic-cancellation methods—just straight SPWM and a properly tuned LC filter—we have a voltage THD of ≈0.22 %. Third- and fifth-order terms at 300 Hz and 500 Hz are reduced below –60 dB, and switching harmonics of higher order near 10 kHz are nicely rejected by the filter. For comparison, IEEE-519 requires voltage THD ≤5 %–8 % for low-voltage grids; our design is over an order of magnitude above this.

IV. Conclusion

This research has been able to show the ability of a single-phase H-bridge inverter, SPWM-controlled at a 10 kHz switching frequency and regulated by a high-speed proportional-integral (PI) voltage feedback loop, to be able to generate consistently a 110 V RMS, 60 Hz AC output from any DC voltage source of equal or greater magnitude than 110 V. One of the most important features of this design is that it operates in linear SPWM mode at a modulation index of approximately 0.62, well below the over-modulation threshold. This keeps the output waveform sinusoidal and unclipped, eliminating the necessity for more advanced modulation schemes like space-vector PWM or harmonic injection.

The inverter uses an LC filter with the components of $L = 4.06$ mH and $C = 6.23\,\mu$F, with realistic parasitic resistances. The configuration achieves a sharp cutoff around 1 kHz, which is effective in attenuating the 10 kHz switching harmonics without significantly affecting the 60 Hz fundamental frequency integrity. The PI controller, optimized for gains $K_p = 21$ and $K_i = 0.03155$, possesses better dynamic performance. It compensates well for voltage oscillations caused by sudden load changes of ±50% and DC-bus disturbances of ±10% in one to two cycles. The worst-case steady-state error obtained is less than ±2%, which is a reflection of robust regulation.

Most significantly, the inverter includes an exceptionally low total harmonic distortion (THD) of

about 0.22% without the use of any sophisticated harmonic compensation methods. Such a level of low distortion is well beyond the needs of most grid-interconnection standards and places the inverter in a position to be used in applications where power quality is of utmost importance. Some examples include renewable energy systems, uninterruptible power supplies (UPS), and sensitive industrial or medical loads.

In the future, a number of strategies would enhance the inverter's performance further. The inclusion of sophisticated modulation techniques such as space-vector PWM or selective harmonic elimination would decrease distortion further or enable more efficient thermal and switching stress management. The inclusion of double-loop control with an inner current loop would enhance transient response dramatically, provide more robust fault management, and enable sophisticated features such as islanding detection for grid-connected systems. Furthermore, switching to higher switching frequencies—20 kHz to 50 kHz—particularly with silicon carbide (SiC) or gallium nitride (GaN) devices, would decrease the size of passive components and increase power density. Lastly, the modeling of real-world losses in power switches and magnetic devices would enable more realistic predictions of thermal and efficiency that are critical to real-world hardware development. In conclusion, this paper validates that a simple full-bridge SPWM inverter, when supported by an optimally designed filter and an adaptive feedback control loop, can meet high standards of power quality and be extremely robust in the face of real-world disturbances, which occur in the field. This offers a solid foundation for further research in academia and field implementation in industry and commerce.

References

C. I. Odeh, A. Lewicki, and M. Morawiec, "A Single-Carrier-Based Pulse-Width Modulation Template for Cascaded H-Bridge Multilevel Inverters," *IEEE Access*, vol. 9, pp. 42182–42191, 2021, doi: 10.1109/ACCESS.2021.3065743.

B. Hemanth Kumar, S. Prabhu, K. Janardhan, V. Arun, and S. Vivekanandan, "A Switched Capacitor-Based Multilevel Boost Inverter for Photovoltaic Applications," *J CIRCUIT SYST COMP*, vol. 32, no. 04, p. 2350057, Mar. 2023, doi: 10.1142/S0218126623500573.

L. Qin, B. Duan, J. L. Soon, W. Hassan, J. Shen, and L. Zhang, "Hybrid PFM and SPWM Control Scheme for DCM Single-Leg-Integrated Boost Inverter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 12, pp. 12288–12298, Dec. 2023, doi: 10.1109/TIE.2023.3236094.

E. H. E. Aboadla, S. Khan, M. H. Habaebi, T. Gunawan, B. A. Hamidah, and M. B. Yaacob, "Effect of modulation index of pulse width modulation inverter on Total Harmonic Distortion for Sinusoidal," in *2016 International Conference on Intelligent Systems Engineering (ICISE)*, Islamabad, Pakistan: IEEE, Jan. 2016, pp. 192–196. doi: 10.1109/INTELSE.2016.7475119.

M. G. M. Abdolrasol, M. A. Hannan, S. M. S. Hussain, and T. S. Ustun, "Optimal PI controller based PSO optimization for PV inverter using SPWM techniques," *Energy Reports*, vol. 8, pp. 1003–1011, Apr. 2022, doi: 10.1016/j.egyr.2021.11.180.

S. K. Yadav, A. Patel, and H. D. Mathur, "PSO-Based Online PI Tuning of UPQC-DG in Real-Time," *IEEE Open J. Power Electron.*, vol. 5, pp. 1419–1431, 2024, doi: 10.1109/OJPEL.2024.3445719.

P. Bistak, M. Huba, D. Vrancic, and S. Chamraz, "IPDT Model-Based Ziegler–Nichols Tuning Generalized to Controllers with Higher-Order Derivatives," *Sensors*, vol. 23, no. 8, p. 3787, Apr. 2023, doi: 10.3390/s23083787.

Y. Peng, W. Sun, and F. Deng, "Internal Model Principle Method to Robust Output Voltage Tracking Control for Single-Phase UPS Inverters With Its SPWM Implementation," *IEEE Transactions on Energy Conversion*, vol. 36, no. 2, pp. 841–852, June 2021, doi: 10.1109/TEC.2020.3030894.

H. Wang *et al.*, "Harmonic Spectra Analysis of Digital SPWM in VSI With DC Bus Ripple and Dead-Time Effects," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9494–9513, Aug. 2023, doi: 10.1109/TPEL.2023.3272381.

B. H. Kumar, M. M. Lokhande, K. R. Reddy, and V. B. Borghate, "An Improved Space Vector Pulse Width Modulation for Nine-Level Asymmetric Cascaded H-Bridge Three-Phase Inverter," *Arab J Sci Eng*, vol. 44, no. 3, pp. 2453–2465, Mar. 2019, doi: 10.1007/s13369-018-3586-3.

J. Soomro, T. D. Memon, and M. A. Shah, "Design and analysis of single phase voltage source inverter using Unipolar and Bipolar pulse width modulation techniques," in *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES)*, Nov. 2016, pp. 277–282. doi: 10.1109/ICAEES.2016.7888052.

J. Sabarad and G. H. Kulkarni, "Comparative analysis of SVPWM and SPWM techniques for multilevel inverter," in *2015 International Conference on Power and Advanced Control Engineering (ICPACE)*, Aug. 2015, pp. 232–237. doi: 10.1109/ICPACE.2015.7274949.

M. Bartoli, A. Reatti, and M. K. Kazimierczuk, *High-frequency models of ferrite core inductorsProceedings of IECON'94 - 20th Annual Conference of IEEE Industrial Electronics*. 1994. doi: 10.1109/IECON.1994.398065.

M. J. Ryan and R. D. Lorenz, "A high performance sine wave inverter controller with capacitor current feedback and 'back-EMF' decoupling," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, June 1995, pp. 507–513 vol.1. doi: 10.1109/PESC.1995.474857.

T. Sakurai and H. Haga, "Power Decoupling Control of Electrolytic Capacitor-Less Dual-Inverter to Reduce Interharmonic Currents Under Periodic Load Fluctuation," *IEEJ Journal of Industry Applications*, vol. 12, no. 5, pp. 990–999, 2023, doi: 10.1541/ieejjia.22011386.

S. Mondal, S. P. Biswas, Md. R. Islam, and S. M. Muyeen, "A Five-Level Switched-Capacitor Based Transformerless Inverter With Boosting Capability for Grid-Tied PV Applications," *IEEE Access*, vol. 11, pp. 12426–12443, 2023, doi: 10.1109/ACCESS.2023.3241927.

S. Ahmad *et al.*, "Direct Power Control Based on Point of Common Coupling Voltage Modulation for Grid-Tied AC Microgrid PV Inverter," *IEEE Access*, vol. 10, pp. 109187–109202, 2022, doi: 10.1109/ACCESS.2022.3213939.

S. Swain and B. Subudhi, "Grid Synchronization of a PV System With Power Quality Disturbances Using Unscented Kalman Filtering," *IEEE Transactions on Sustainable Energy*, vol. 10, no. 3, pp. 1240–1247, July 2019, doi: 10.1109/TSTE.2018.2864822.

H. Wu, S.-C. Wong, C. K. Tse, and Q. Chen, "Control and Modulation of Bidirectional Single-Phase AC–DC Three-Phase-Leg SPWM Converters With Active Power Decoupling and Minimal Storage Capacitance," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4226–4240, June 2016, doi: 10.1109/TPEL.2015.2477504.