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Design Of Circuit Compatible Model For Carbon Nanotube Field Effect Transistor

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Abstract

Device scaling drives technological advancements, but CMOS technology faces imminent limitations. To extend its functionality and explore new device paradigms, alternative nanoscale devices are being investigated under the 'More than Moore' approach. This trend integrates functionalities that do not scale according to Moore's law. Emerging devices such as FinFET, Tunnel FET, Junction-less FET, Tri-gate, Si-nanowire MOSFETs, Carbon-based FETs, and Spin-FETs are being explored. To incorporate these devices into circuit simulations, equivalent models must be developed since conventional models cannot accurately represent nanoscale behavior. This study presents a compact model for Carbon Nanotube Field-Effect Transistors (CNTFETs) for circuit simulations. Carbon nanotubes (CNTs) have gained significant academic interest due to their unique electrical properties, including ballistic and non-ballistic electron transport. CNTFETs offer advantages such as mechanical strength, flexibility, low power consumption, thermal stability, and high circuit density. Initially, the OPV molecule—considered part of a graphene sheet—will be analyzed before extending the model to CNTs, which are essentially rolled-up graphene sheets. Current CNT transistor modeling techniques primarily use MATLAB to simulate transport mechanisms. These models rely on ideal numerical equations, often failing to account for non-ballistic transport effects, resulting in discrepancies between simulations and real-world performance. The primary goal of CNT transistor modeling is to predict circuit performance before fabrication, ensuring simulation results closely reflect actual device behavior. This work develops a simple compact model that accurately reproduces CNTFET I–V characteristics using the Non-Equilibrium Green's Function (NEGF) approach. By leveraging NEGF, the model

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bypasses complex density function tight-binding calculations, facilitating efficient I–V characterization and improving the integration of CNTFETs in circuit simulations.

Keywords: Carbon Nanotube Field-Effect Transistor (CNTFET), Compact Modeling, Non-Equilibrium Green's Function (NEGF), Circuit Simulation, Nanoelectronic Devices

Introduction

Carbon nanotube (CNT) was discovered by Iijima in 1991[1], this new type of material continues to attract attention for its great potential to be applied as metallic nanowires and active semiconductor devices in next generation integrated circuits (ICs). Net worthy progress has been attained in terms of both understanding the major electronic properties and discovering possible engineering applications of CNTs [2].After the exploration of first CNTFET many other Nano electronic devices have been comprehensively explored [3]. CNT based transistors have been demonstrated both theoretically and experimentally. The transport characteristics of CNTs have been considered to be of significant importance for a CNT based transistor and thus have been widely studied. Ideally, for a carbon nanotube with its length much shorter than the mean free path of conduction electrons, a ballistic regime is generally exhibited in the nanotube [4]. However, the transport mechanism of CNT transistors is complicated and the extensive existence of non-idealities may result in non-ballistic transport. The carbon nanotube may have ballistic or non-ballistic transport which depends on energy region, on which the theoretical analysis of CNT transistors should be focused.

The modelling of carbon nanotube devices, especially CNT transistors, has been developed significantly during the past several years. A number of

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transistor models have been projected in both experimental and theoretical studies. To understand the operation mechanisms of CNT transistors, significant progress has been made. Early research demonstrated that CNT transistors operate like metal-oxide-semiconductor field effect transistors (MOSFETs) [5, 6] or Schottky-barrier (SB) transistors [7]. Nevertheless, as more electronic characteristics of CNT devices are revealed, both behavioural level and circuit-level models have recently emerged and been applied into the simulation of CNT logic circuits [8]. Common techniques for modelling CNT transistors depend on the l evaluation of Newton-Raphson iterations in the energy domain within the nanotube or evaluation of integrals to get solutions of non-linear dependencies [9], which encounter calculation complexities and are consequently time-consuming. Additionally, early CNT transistor models can only describe ideal ballistic transport properties and are not sufficient for practical use. Recently, new techniques which use symbolic approximation of mobile charge densities [10] and count in sub-band effects of CNTs [11] have been developed to improve the efficiency and availability of the models. Though great efforts have been made, CNT transistor models are still being developed and novel methodologies remain to be identified. Similarly to the development of most electronic device models, simulation is required in to address questions in the rapidly growing field of modelling CNT transistors [12].

Currently, most CNT transistor models describe the DC transport characteristics within the channel, and simulation can be made to numerically identify the relations between different parameters and the flow of carriers through the carbon nanotube channel, which verify the performance of the proposed models and help to optimise them [13]. A number of theoretical CNT transistor models [14] have been developed,

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which derive ideal ballistic output results in simulation but consume much CPU resource, and are thus not efficient enough for practical use. Therefore, novel numerical modelling techniques are needed to shorten the simulation periods without losing much accuracy, especially when applied to circuits. Although numerical modelling techniques have recently been proposed [15], the simulation results diverge and there is a lack of comparisons with experiments. In the light of non-idealities (defects, misalignment, etc.) of CNTs, the proposed models are required to be able to reflect these non-ideal effects on the transport characteristics of CNT transistors in simulation. The performance of the proposed models also needs to be compared with results obtained from both numerical analysis and experiments. Both theoretical analysis of the electronic properties of CNT transistor and improvement of the modelling techniques are needed.

Carbon Nanotube Transistor Modelling

Semiconducting carbon nanotubes have impressive electronic features and as a result are promising new material for the next generation of ICs. CNT transistors have been constructed experimentally and their performance has been demonstrated to exceed conventional silicon FETs [16]. Furthermore, the need for developing models which can describe the characteristics of CNT transistors is increasing. A number of current techniques for CNT transistor modelling employ MATLAB to numerically present the transport mechanism [17, 18, 19]. In numerical models, the electronic parameters of CNT transistors are quantified and the relationships between the inner components are also represented by mathematical equations. However, these models are based on ideal numerical equations and their performance in practice differs from that obtained in simulation since the non-ballistic transport characteristics of

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transistors are not included in the proposed numerical models. Most recently reported models are based on numerically describing the transport characteristics of CNTs [19, 20, 21], which implies the importance of revealing the electronic mechanism of the nanotube. Although some theories have been suggested, there are still some phenomena that need theoretical explanation. For example, the doping mechanism of CNTs is quite different from silicon and plays important role in the mobility of the nanotube. This can explain why most existing models are focused on the ballistic transport characteristics. Recently symbolic approximation for modelling charge densities in the ballistic region of a CNT transistor has been presented [11, 22]. The approximation technique permits a fast and accurate calculation of the charge densities within the CNT channel, which presents a closed-form solution to drain-source current in a CNT channel in the form of function of parameters including temperature, terminal voltages, Fermi level, and CNT diameter of the transistor. The aim of modelling CNT transistors is to predict the performance of circuits with CNT devices by running simulation before fabrication, expecting that the simulation results can reflect the performance of real devices. At present there exists a gap between experimental and simulation results. One reason is that the electronic mechanism of CNTs are yet to be established; another reason is that the fabrication of CNT transistors is difficult to control and no uniform results are obtained from various experiments, which implies that feasible approaches to fabricating CNTs are still under development.

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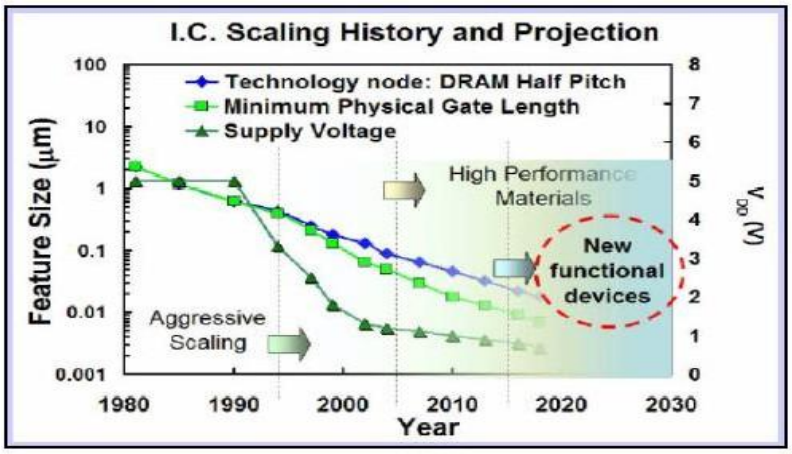

Figure 1: IC Technology Propagation [25]

MOSFET Scaling

Transistor scaling is predicted by Moore's law. The number of transistors on one IC chip has quadrupled every three years and the dimensions of each transistor has narrowed [24]. Sustainable device scaling is necessary to maintain sequential improvements in IC technology [25]. Classically, the scale is guided by some approaches that have specific application objectives in mind. Based on the supposition (1) to minimize the dimensions of the device by improving the lithography, and (2) the stability of the MOS structure, the scaling laws can be classified into several groups. Among these constant field scaling (CFS), constant voltage scaling (CVS), quasi constant voltage scaling (QCVS) and generalized scaling (GS) take the main place. This is summarized in Table 1.

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Table 1: Scaling laws on MOSFET Devices [25]

Parameter	Notation	Constant-Field	Generalized-Field	Constant Voltage
Dimensions	W,L,	$1/\lambda$	$1/\lambda$	$1/\lambda$
Doping			$^{2}/$	$^{2}/1$
Applied Voltage	V_{DD}, V_{th}	$1/\lambda$	$1/k$	1
Electric Field		1	λ/k	
Current		$1/\lambda$	λ/k^2	
Capacitance	$= \frac{\varepsilon_r \varepsilon_0 A}{d}$	$1/\lambda$	$1/\lambda$	$1/\lambda$
Power		$1/\lambda^2$	$1/k_\lambda$	$1/\lambda$
Delay		$1/\lambda$	k/λ^2	$1/\lambda^2$

Limitations Of Mosfet Miniaturization

Upon reaching nanometer scale of MOSFET we come across many factors that effects its performance.

Short Channel Effect

The short channel offers several MOSFET leakage methods such as low inversion current, reverse-bias p-n, and barrier lowering induced by drain [26]. The DIBL (Drain induced barrier lowering) current occurs when the potential source barrier decreases due to the interaction of the drain area with the source. The presence of DIBL will reduce the Vth. The GIDL in the high electric field occurs between gate and drain, as happens along the width of the channel between the gate and the drain.

Tunneling Limit

Normally in the operating system or computing, the transistors are adequately integrated enough that the operation of the transistor is not

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interfered by another. The separation is done by adding a material acting as a barrier between them. But the barriers also become thin when the low-impedance circuits are low. That's why there exist a possibility that one MOSFET carrier is crossing another and results in performance distortion. This effect grows significantly when barrier distance decreases [10].

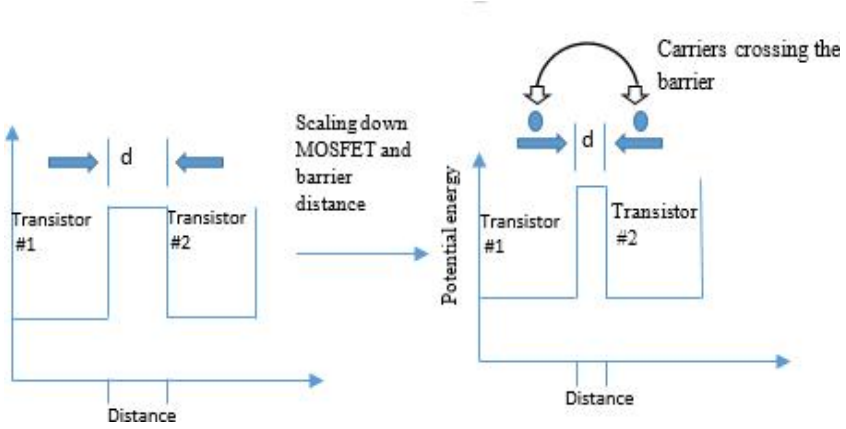

Figure 2: Potential barrier between two transistors.

Threshold Voltage Effect

There are significant limitations on the MOSFET that the does not decrease proportionally with respect to the scaling of transistor. The remains constant when length of the channel is between 1µm-0.1µm and further deviates when the channel length is less than 0.1µm [27]. If the transistor is reduced to less than 0.1µm, the voltage-current will not immediately reach down to zero, but it will invariably reduce inversely with thermal energy [10].

Oxide Thickness

Gate thickening caused two types of constraints. First, a thin layer of oxide increases the current leakage. This is related to the effect of the quantum tunneling controlled by the MOSFET when reducing the thickness of the oxide. Second, because of the thickness of the oxide, there is a loss of

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inversion charge as well as a trans-conductance due to the quantification of the inversion layer and the effect of the polysilicon gate depletion. [15] Some other limitation factors also seem in terms of scaling down of MOSFET:

Theoretical Limitation

Thermal limit, quantum limits and power dissipation, these are three important limitations that are usually considered theoretical constraints. The energy required to write should be higher than the thermal function in order to avoid a bit error. This is known as thermal limit.

Design Limitation

Scaling down MOSFET detects its limits from the current design. The limit is because of the reason that the Zener breakdown at the junction of the source/substrate [28]. As leakage begins at the gate becomes very difficult to control the channel.

Power Consumption and Dissipation

Energy consumption and heat dissipation are one of the hurdles to further progress in Silicon based transistors. A large amount of energy consumption promotes heat generation, which increases the risk that transistors will interfere with each other.

Alternative Structures and Materials

As the size of the devices approaches the nanometer, new breakthroughs arise from harnessing the properties of the nanometer. The chemical composition, self-assembly, and self-assembly of fabrication is by accurately synthesizing hardware structures or whole functional entity. New devices encapsulating dimensional transport and quantum phenomenon can lead to different trade-offs between power and performance. Other new materials with new properties appear as a result of their ability to

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process the material on a nanometer. Therefore it is possible to think of new Nano electronic structures built on novel devices, for example, nanowires, molecular devices, Nanotubes and novel device concepts for nanotechnology. A few other techniques such as mobility enhancement, metal gates with high dielectric insulations, optimal doping profile design, a vertical channel transistor, etc., were proposed [29]. In addition to new silicon device manufacturing techniques, various materials, such as gallium arsenide, were considered substitutes for silicon [30]. One of these substances is graphene, which is a single layer of carbon atoms arranged in a hexagonal pattern.

OPE Molecular Analysis

Using organic molecules in Nano-electronic devices is one of the ultimate goals in nanotechnology. To attain this it is necessary to control, measure and understand charge transport through molecule junctions and amendment in structures toward desired functionalities through molecules attached to electrodes. The conductive properties of Nano-devices are sensitive to molecular interconnects and the capacitive coupling between molecules and electrodes.

Before proceeding to CNTFET's, in our work we explore the charge transport characteristics of fixed number of OligoPhenylene Ethynylene (OPE) molecules attached to gold electrodes. Because OPE is also a layer of graphene sheet which is when rolled in a specific pattern leads to structure of carbon nanotube. Therefore initial analysis is done on OPE structure. The analysis of OPE molecules using non-equilibrium Green's function formalism and first-principle density functional theory is done. Further, our calculations are based on the I–V characteristics, In particular, we observed the relation between junction conductance and overlapping of molecular

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orbitals. By varying parameters like the horizontal and vertical distances (gap), and tuned the electronic response of the system. We finally proposed a generic optimized molecular arrangements considered for studying
The electrical transport properties .This Perspective elaborates on the distance and reflects on the effect of distance on conductance herein, we address the question what happens when is applied.

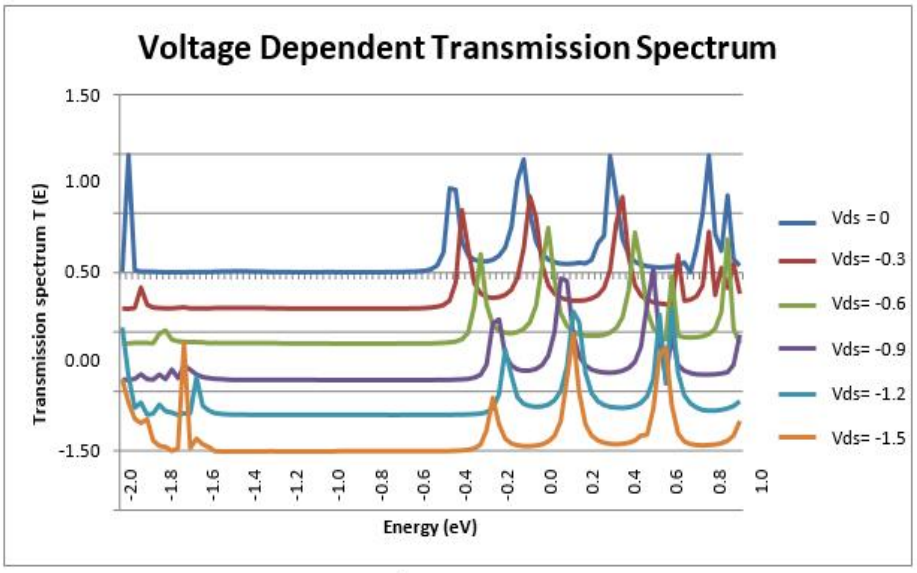

Figure 3: Transmission spectrum of OPE

Peaks in Transmission spectrum represents molecular orbitals, which are responsible for electron transport. Fermi level tries to cross molecular orbital near zero due to self- consistent field effect which is known as quantum mechanical effect. In Figure 3 we see shift towards higher energy level, so electron do not find room for any transport. This effect is not prominent in bulky devices. Energy gap is dependent on external applied voltages which are gate voltage and drain to source voltage.

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Introduction to Carbon Nanotubes

Carbon nanotubes are 1-D molecular structures which are obtained as a result of the folding of a graphite (hexagonal carbon network) in a cylinder. It may be of single shell, single walled nanotubes (SWNT) or multiple shells, multi-walled nanotubes (MWNT).

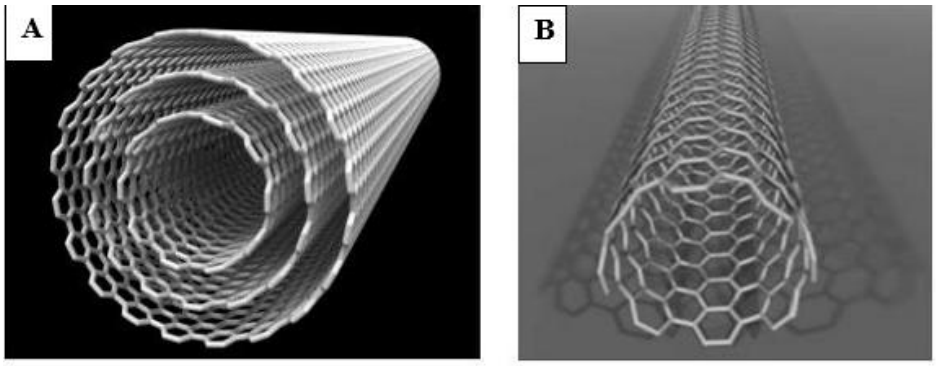

Figure 4 Carbon nanotubes: (a) Multiwalled carbon nanotubes (MWCNT) and (b) Single-walled carbon nanotubes (SWCNT) [22]

The nanotube can be seen as a wrapped graphene sheet. To understand the properties carbon nanotubes it is needed to understand electrical characteristics of graphene sheet. Graphene is defined as a two-dimensional zero-gap semiconductor [25]; for many directions in this sheet, there exists a gap in the range, and the electrons cannot flow along this gap unless additional energy is applied. However, in some special directions (with a zero gap), graphene is a metal, and the electrons flow freely through these directions. To make a nanotube from graphene sheet, a special direction is determined, which is the direction along the axis of the nanotube. Depending on this trend, metal and semiconductor nanotubes can be obtained [31].

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Carbon Nanotube Characteristics

Carbon nanotubes, as new materials with unique electronic properties, are expected to be used to manufacture electronic devices for their physical properties better than those found in traditional silicon, for example, longer mean free path, larger carrier mobility and higher transport current density.

Electrical Properties of Different Types of CNT's

In light of transport conductivity, carbon nanotubes can be classified as metallic or semi- conducting carbon nanotubes [32], determined by the energy gap between the atoms. The type of conduction depends on its chirality [27]. Both metallic and semiconducting CNTs have been studied as potential electronic components and their electronic properties have been established.

Metallic CNTS's

Devices made of SWCNTs were first measured in 1997 [33] and have been extensively studied since then. The conductance of metallic SWCNTs is varied greatly at room temperature [24]. Much of this contradiction is due to a change in the resistance of the contact between the electrodes and the tube [25]. The conductivity of metallic nanotubes can be equal or even exceed, delivering the best metals at room temperature [26].

Semiconductor CNT's

Semiconductor carbon nanotubes can be derived by choosing the specific shape of the nanotubes. Electrons pass through semiconductor nanotubes even at Fermi's energy due to contact effect. As the length of the nanotube increases, this effect decreases and shows a gap like structure. The carrier mobility and the mean free path of semiconductor carbon nanotubes have been shown to be correlated with temperature and tube chirality. Both fall when the lattice temperature rises. Semiconducting carbon nanotubes have

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proved to be potential applications in high-mobility electronic devices [34], indicating that they are highly semiconducting. In this work we are using Semiconducting CNT.

Electron Mobility Characteristics in CNT

Single-walled carbon nanotubes are potential in electronics applications because of their semiconducting and metallic properties, and their ability to achieve high current rates. Electrons and holes have a high current density along the CNT channel due to low dispersion rates along the CNT axis. This type of structure looks like an ideal waveguide. When the electron or hole moves along the CNT metallic or semiconducting axis, the scattering rates are minimal. The carbon nanometer scatters lengths are found on the micrometer length scale, while the related electron distances are in the nanometer range. This is due to the limited number of impurities and defects in the structure of carbon nanotubes, and the absence of interface problems due to saturated and stable chemical bonds forming CNT. Atomic wave vectors create circular standing waves around the core and restrict electrons and holes in travel only in the axial direction. The stable and saturated carbon-carbon bonds also limit electrical migration in nanotubes. CNTs can carry current around 10 pA/nm2, but normal metal wires current carrying capability is around 10 nA/nm2. Thus, carbon nanotubes have the ideal current capacity: substantial mobility and high electro migration thresholds.

Carrier's Density

The density of carriers (electrons or holes) is a central characteristic of semiconductors. This is the total number of occupied states in the sub band. Here in this subject, we focus on electron carrier density and the results

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apply well to the holes due to electron-hole symmetry in the CNT scale structure. The electron carrier density is given as follows:

$$n_{CNT} = \sum_{p=1}^{p} \left[\int_{E(0,p)}^{\infty} D(E) f(E, \mu_f) dE \right] \quad \text{.....2.1}$$

Where p is number of sub band, $E(0, p)$ is lowest energy of each pth sub band, $D(E)$ is density of state, $f(E, \mu f)$ is Fermi Dirac distribution function and μf is Fermi level

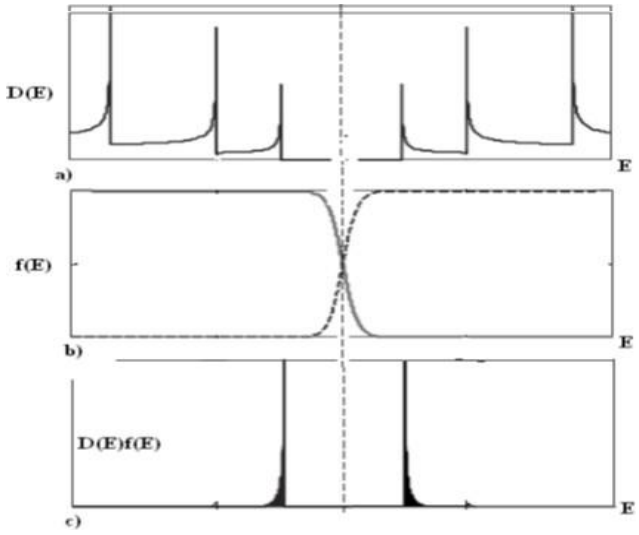

Figure 5 Contribution of First two Sub-bands to Carrier Density relative to higher Sub-bands [35]

Figure 2.5 Illustrates contribution of first two sub-bands to carrier density relative to higher sub-bands (a) DOS (b) f (E) for electrons (solid) and holes (dashed). (c) DOS multiplied by the Fermi–Dirac function showing only the first sub-band contributes appreciably to carrier density at equilibrium [26]. Equation 2.1 takes into account all sub-bands. However, the Fermi Dirac distribution function rapidly decomposes to higher energies [27]. Therefore,

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we can only take the first two sub-bands to apply the (V1) without loss of accuracy. Hence, equation 2.1 is rewritten as follows:

$$n_{CNT} = \sum_{p=1}^{2} \left[\int_{E_{(0,p)}}^{\infty} D(E) f(E, \mu_f) dE \right] \quad \text{..... 2.2}$$

Carbon Nanotube Field Effect Transistor

The possibility of achieving Nano scale transistors using individual semiconductor semiconducting carbon nanotubes offers potential as an alternative to silicon technology beyond Conventional measurement limits. The major challenge is to achieve low-voltage nanotube transistors, which exhibit a good trans-conductance, steep sub threshold swing, and large on/off ratio. It is still necessary to prove their assimilation into the circuits with high signal gain and good stability.

It has been recently demonstrated [36] that these goals can be accomplished with the help of a bottom gate device structure that incorporates patterned metal gates with a thin gate dielectric based on a self-assembled molecular monolayer. The transistors obtained operates on a source voltage of 1 volt and have a 5µS Trans conductance, a sub threshold swing of 68mV/decade, and an on/off ratio of 107. It is also verified that the device structure can be applied to the implementation of unipolar logic circuits Good switching performance [37].

Most proposed structures consist of a CNT channel and metal terminals as gate, source and drain, and the contacts may influence the performance of the devices. Reports have presented that the formation of ohmic contact between individual SWCNT and Pd electrode was achieved by applying the pulsed voltage of several volts for microseconds in the Pd

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electrode [19]. Novel high-k materials make it practical to model Nano-scale transistors, which tends to push the performance limit for molecular electronics. SWCNT transistors with integrated ZrO2 high-k dielectrics have been reported [38]. Additionally, high performance enhancement mode CNT transistors have been obtained using high-_ HfO2 films as gate insulators [39], in which excellent OFF states to nanotube FETs under aggressive vertical scaling can be derived. Polymer electrolytes have also been demonstrated as gate media to construct CNT transistors showing high on-state conductance, carrier mobilities and on-off ratios [26].

Structure of CNTFET

CNTFET was announced in 1998. Initially they were simple devices fabricated by depositing single-wall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been pre patterned with gold or platinum electrodes. Nanotube channel was connected through electrodes which were source and drain. Its schematic is shown in Figure 6, observed transistor action was of p-type, with modulation of the over several orders of magnitude. The devices demonstrated high on-state resistance, low trans-conductance but there was no current saturation, and they needed high gate voltages to turn them on.

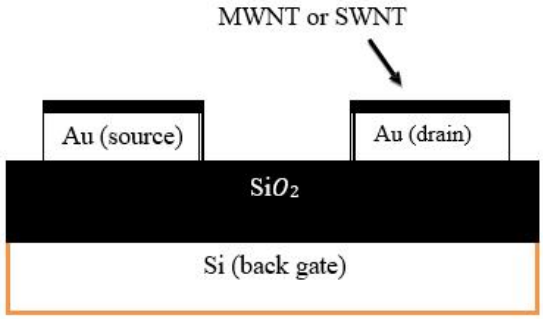

Figure 6: Early CNTFET Structure [40]

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Based on those initial CNTFET results improvements in CNTFET device structures and processing bore much advancement in their electrical properties. As a substitute, laying the nanotube down upon the source and drain electrodes, the electrodes were patterned on top of previously laid down CNs. Other than Au, Ti and CO were used to improve the metal/nanotube contact.

Operation of CNTFET

CNFET and MOSFET follow similar basic principle of operation, electrons are supplied by source terminal and collected by drain terminal. Gate terminal shifts current intensity and with no gate voltage the transistor is in Of-state. Below is discussed the operation of MOSFET-like structure.

MOSFET like CNTFET

Unlike SB-CNTFET, MOSFET-like CNTFET displays unipolar behaviour by suppressing either electron (for p-type) or hole (for n-type) transport. The structure of MOSFET-like CNTFET consists of two un-gated portions that are heavily (n++/p++) or lightly (n/p) doped as shown in Figure 7 (a).

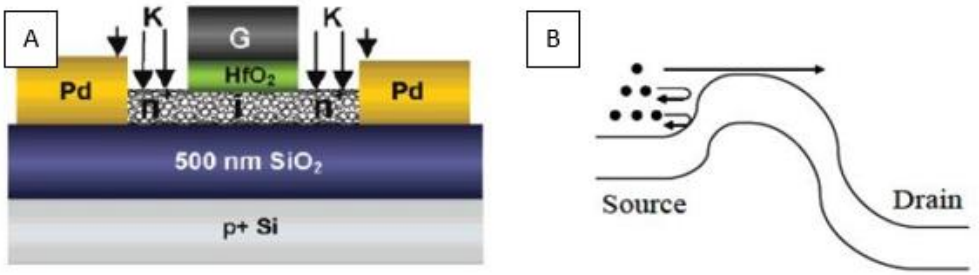

Figure 7: (a) The Structure of MOSFET-like CNTFET; Ungated Regions are Doped with K (potassium) to Form N-type CNTFET [17], b) Operation Mechanism of MOSFET-like CNTFET [17].

The non-tunneling potential barrier, as shown in Figure 7, in the channel region and thereby the conductivity is modulated by the gate-source bias.

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Charge restricts the on- current as shown in Figure 8. Charge induced by gate voltage controls the drain current.

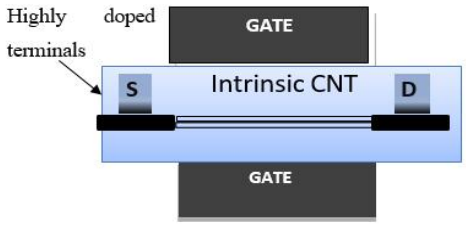

Figure 8: MOSFET-like CNTFET Structure

This type of transistor provides longer channel length limit because of reduction in metal induces gap states which results in faster operation of the transistor.

Silicon has played a fundamental role in the semiconductor industry, forming the basis of most semiconductor device models. Traditional semiconductor devices have undergone significant advancements over the past decades, driven by the unique transport characteristics of semiconductors, which are influenced by factors such as temperature and light. A crucial component of semiconductor devices is the p-n junction, formed by combining p-type and n-type semiconductors. This structure is widely utilized in modern electronics, particularly in diodes, where current flows from the p-type to the n-type but not in the reverse direction. Other key semiconductor devices include bipolar junction transistors (BJTs), which involve both hole and electron conduction, and field-effect transistors (FETs), which rely on an electric field to control conductivity. Metal-oxide-semiconductor field-effect transistors (MOSFETs) are developed by depositing a silicon dioxide (SiO_2) layer and a metal layer onto a semiconductor substrate. In MOSFETs, the source and drain are connected by a conductive channel, and both regions must be of the same type.

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MOSFET technology has experienced significant scaling down in recent years, with the Si-SiO_2 interface remaining a crucial element. The motivation behind MOSFET scaling is to enhance device performance, but challenges such as fabrication complexities and low-voltage operation persist.

The potential of carbon nanotube (CNT) devices in electronics has gained considerable attention due to their unique electronic properties. Researchers have explored the feasibility of constructing semiconductor devices and circuits using semiconducting CNTs. Circuit-level CNT transistor models have been developed to characterize the macroscopic behavior of CNT field-effect transistors (CNTFETs). Researchers at Stanford University have implemented a circuit-compatible SPICE model for enhancement-mode CNTFETs, which exhibits real-time dynamic response. Similarly, researchers at Purdue University have developed a MATLAB-based model to evaluate CNTFET performance, particularly the current-voltage (I-V) relationship. Various equivalent circuit models have been introduced to simulate CNTFET behavior, including a ballistic one-dimensional CNTFET model that correlates device characteristics with applied terminal voltages. However, the accuracy of such models is limited under high-bias conditions. Another advanced circuit-compatible model incorporates gate-substrate coupling capacitance, trans-capacitance pairs, and quantum inductance, which influence high-frequency performance. These models indicate that enhancement-mode CNTFETs are suitable for circuit applications due to their fabrication feasibility and superior device characteristics.

Researchers have also investigated the density of states and band structure of CNTs using various methodologies, including finite integration, Newton-Raphson iteration, and non-equilibrium Green's function approaches. These studies have demonstrated that the energy band of

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CNTFETs is influenced by external terminal voltages, and ongoing research aims to simplify numerical calculations related to CNT transistor channel currents. Analytical modeling equations have been developed to describe current transport in CNTFETs, highlighting the strong dependence of performance on device geometries. Another significant area of research focuses on eliminating the influence of metallic CNTs in semiconducting CNT devices. A single stuck-at fault method has been proposed to model and detect metallic CNT defects, while a mathematical algorithm utilizing CNT diameter and chirality has been shown to effectively distinguish between metallic and semiconducting CNTs. Temperature also plays a critical role in CNTFET modeling, as it affects the energy band and carrier density within the transistor channel.

A theoretical ballistic CNT model has been introduced to explore two-dimensional electrostatic effects and self-consistent potential in CNT transistors. This model suggests that the self-consistent potential in the gate region governs carrier transport within CNTFETs. The self-consistent voltage, a newly introduced concept, explains how the CNT energy band is influenced by external terminal voltages. The model integrates non-equilibrium Green's function formalism and the numerical solution of the Boltzmann equation to provide a comprehensive mathematical representation of CNTFET operation. A two-dimensional ballistic MOSFET-like model has also been developed, incorporating four capacitors to account for the impact of terminal voltages on barrier potential. The mobile charge distribution in CNT transistors is determined by factors such as source and drain Fermi levels, self-consistent potential, and applied bias voltages. Solving the governing equation for self-consistent voltage typically involves iterative techniques, such as the Newton-Raphson

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method, which enables accurate modeling of ballistic transport characteristics. However, the iterative nature of this approach impacts computational efficiency. Recent research has aimed at improving CNT transistor modeling by addressing limitations in numerical calculations and enhancing the predictive accuracy of CNTFET behavior. Furthermore, studies on CNTFETs have compared different device models, such as Schottky barrier-, conventional-, and tunneling-CNTFETs, with findings suggesting that tunneling-CNTFETs offer advantages in power consumption and performance. Additionally, research has been conducted on high-k dielectric gate capacitance models for CNTFETs, demonstrating their applicability across various CNT diameters and one-dimensional semiconductor devices.

Overall, the ongoing advancements in CNT device modeling continue to refine the understanding of CNT transistors' electronic properties, enhancing their potential application in next-generation semiconductor technologies.

Transport Mechanism in Carbon Nanotube

For analyzing the energy characteristics of a device, it is crucial to determine the conduction and valence band profiles along the transverse direction of the device. This results in an energy versus position plot, known as an energy band diagram, which helps identify properties such as the band gap—the energy required to move an electron from the valence to the conduction band. As device dimensions shrink, the wavelength of carriers becomes comparable to the device dimensions, leading to carrier behavior analogous to a wave on a bound string. The band structure is derived from a unit cell of a periodic crystal and provides insight into the potential properties of nanoscale devices based on their material

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composition. One of the critical properties inferred from the band structure is conductivity. If the conduction and valence bands overlap at any point in the band structure, the material exhibits metallic behavior, making it suitable for use as an interconnect. Otherwise, if a band gap exists, the material is semiconducting and may serve as a channel material for a field-effect transistor (FET). This distinction is particularly relevant to carbon nanotubes (CNTs), which can exist in both metallic and semiconducting forms, as demonstrated by their respective band structures.

Tight Binding Method

The Density Functional Tight Binding (DFTB) method is based on the linear combination of atomic orbitals (LCAO) approach. It is a computationally efficient technique for calculating electronic band structures using wave functions and has been widely employed to study the behavior of carbon-based materials, including CNTs. DFTB provides a suitable framework for analyzing transport properties, making it a valuable tool in semiconductor research.

The Non-Equilibrium Green's Function (NEGF) Formalism

Proposed by Martin Schwinger in 1959, the NEGF formalism is widely used for simulating quantum transport in molecular devices. It solves the Schrödinger equation under non-equilibrium conditions, serving as the foundation for quantum device simulations. In the NEGF approach, a device is represented by a Hamiltonian (H) coupled to the source and drain, which are characterized by their respective Fermi levels, μ_S and μ_D. The coupling between the device and the source/drain is described using self-energy matrices (Σ_S and Σ_D). Once the Hamiltonian and self-energy matrices are obtained, the electron density matrix and transmission coefficient at a given energy level are computed, followed by numerical

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integration over the energy space to determine the electron density and terminal currents.

The NEGF approach consists of several steps. The first step involves selecting a basis set and constructing the Hamiltonian matrix for the channel, incorporating the self-consistent potential. The second step calculates energy matrices Σ_S, Σ_D, and Σ_C, which describe the coupling between the channel and the source/drain. The third step computes the Green's function using the equation $G(E) = [(E + i0+)I - H - \Sigma_S - \Sigma_D]^{-1}$. Finally, physical quantities of interest, such as charge density and current, are derived from the Green's function. The electronic charge (e) and charge neutrality level (E_N) are fundamental parameters in these calculations. The total charge in the system is given by the equation $Q(Z) = Q_S(z) + Q_D(z)$, while the drain current is calculated using the equation $I = (4e/h) \int T(E) [f_S(E) - f_D(E)] dE$, where T(E) represents the transmission probability between the source and drain.

Hamiltonian and Quantum Transport

To compute the Green's function, an appropriate Hamiltonian must be defined. For infinite, periodic structures, Bloch's theorem and the tight-binding approximation are commonly used, while for finite or semi-infinite crystals, the Hückel approach provides a suitable alternative. The Hückel Hamiltonian closely resembles the tight-binding Hamiltonian and is particularly useful for modeling CNT structures. In a discretized form, the Green's function equation, without self-energies, is given by $G\pm = \lim[(E \pm i\xi)I - H]^{-1}$, where ξ approaches zero. The Hamiltonian matrix for CNTs exhibits a periodic diagonal structure, with local potential energy values determining its elements.

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Transport Mechanism in CNTFETs

The transport mechanism in carbon nanotube field-effect transistors (CNTFETs) is inherently one-dimensional. The relationship between transport and gate voltage can be observed under different gate field conditions. When the gate voltage (V_G) is below the threshold voltage (V_{th}), the transistor remains in an off-state, with minimal conduction. As V_G increases beyond V_{th}, the valence band in the channel region starts overlapping with the source region's Fermi level, leading to charge accumulation and a shift in band movement. This phenomenon reduces barrier thickness and enhances tunneling current. However, once the charge accumulation reaches a certain point, the tunneling current saturates as the barrier thickness stabilizes.

Charge Transport and Self-Consistent Solutions

Under equilibrium conditions with no net charge flow and $V_{DS} = 0$, the carrier distribution follows the Fermi function. When a gate voltage is applied, band bending occurs in the mid-length region of the device, causing the conduction band edge (E_C) to shift relative to the fixed Fermi level (E_F). A self-consistent solution for the system is obtained by solving Poisson's equation, which describes charge distribution as $Q_v(z) = q(p - n) = q \int g(E) \{f(E + qV_{CS}(z)) - f(E - qV_{CS}(z))\} dE$. Here, $g(E)$ represents the tight-binding density of states, $f(E)$ is the Fermi function, and $V_{CS}(z)$ denotes the band-bending potential.

Ballistic Transport in CNTFETs

Ballistic transport is expected in CNTFETs due to their nanoscale dimensions and the applied voltage conditions. Under the Landauer-Büttiker formalism, the device is treated as a system composed of reservoirs separated by a transport region, characterized by a transmission probability function $T(E)$.

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Each region follows its own equilibrium carrier statistics f(E). The standard electron current expression I = -qnv accounts for the energy-dependent transport properties. The current between the source and drain is calculated as I = (-2q/h) ∫ [f_S(E) – f_D(E)] T(E) dE, where μ_S and μ_D represent the source and drain Fermi levels, respectively. The transmission coefficient T(E) is a function of device parameters, while the Fermi functions depend on the contact Fermi energies, which are influenced by the drain-source voltage (V_DS).

Overall, understanding transport mechanisms in CNTFETs is essential for optimizing their electronic performance. By leveraging tight-binding methods, NEGF formalism, and Hamiltonian models, researchers continue to refine CNTFET modeling techniques, enabling improved predictions of device behavior and potential applications in next-generation semiconductor technology.

Results

Model Derivation

Two MATLAB models were developed in this research to simulate the current-voltage (I-V) characteristics of a Carbon Nanotube Field-Effect Transistor (CNTFET). The overall CNTFET model is constructed based on theoretical knowledge of CNTFETs and experimental I-V measurements. This research focuses on a simulation-based study to investigate the impact of varying different parameters on the I-V characteristics of CNTFETs.

Model 1: Physics and Calculation Process

In Model 1, when a positive voltage is applied between the drain and source $(V_{DS} > 0V)$, the current remains constant along the CNT due to ballistic transport and can be determined at the start of the channel. Electrons from the drain occupy energy levels with negative wave numbers, while electrons

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from the source occupy energy levels with positive wave numbers. The conduction band decreases by $^{qV_{CNT}}$ when a positive $^{V_{DS}}$ is applied, where $^{V_{CNT}}$ epresents the CNT surface potential. When a gate-source voltage $^{(V_{GS} > 0V)}$ is applied, the conduction band at the channel decreases by $^{qV_{CNT}}$ because each sub-band decreases by the same amount along the entire channel length. The drain current for each sub-band can be calculated using the Landauer formula:

In Model 1, when a positive voltage is applied between the drain and source $^{(V_{DS} > 0V),}$ the current remains constant along the CNT due to ballistic transport and can be determined at the start of the channel. Electrons from the drain occupy energy levels with negative wave numbers, while electrons from the source occupy energy levels with positive wave numbers. The conduction band decreases by $^{qV_{CNT}}$ when a positive $^{V_{DS}}$ is applied, where $^{V_{CNT}}$ epresents the CNT surface potential. When a gate-source voltage $^{(V_{GS} > 0V)}$ is applied, the conduction band at the channel decreases by $^{qV_{CNT}}$ because each sub-band decreases by the same amount along the entire channel length. The drain current for each sub-band can be calculated using the Landauer formula:

$$I_{DSP} = \frac{4qkT}{h}[\ln(1 + e^{\xi_{Sp}}) - \ln(1 + e^{\xi_{Dp}})]$$

Where, T is temperature, k is the Boltzmann constant, and $\hbar$ is Planck's constant. The variables ξSp and ξDp are defined as:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT}, \quad \xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT}$$

Where, ECp represents the conduction band minima for sub-bands. The total drain current is obtained by summing the contributions of all sub-bands:

$$I_{DS} = \frac{4qkT}{h} \sum_{p} [\ln(1 + e^{\xi_{Sp}}) - \ln(1 + e^{\xi_{Dp}})]$$

The surface potential, $VCNT$, is evaluated using the following approximation

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$$V_{CNT} = \begin{cases} V_{GS}, & \text{for } V_{GS} < \frac{E_C}{q} \\ V_{GS} - \alpha(V_{GS} - \frac{E_C}{q}), & \text{for } V_{GS} \geq \frac{E_C}{q} \end{cases}$$

Where, EC is the conduction band minima for the first sub-band, and the parameter α depends on VDS is given by:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2$$

Where, α0=0.79, α1=−0.21 and α2=0.07. The IV characteristics of Model 1 are depicted in Figure 5.1

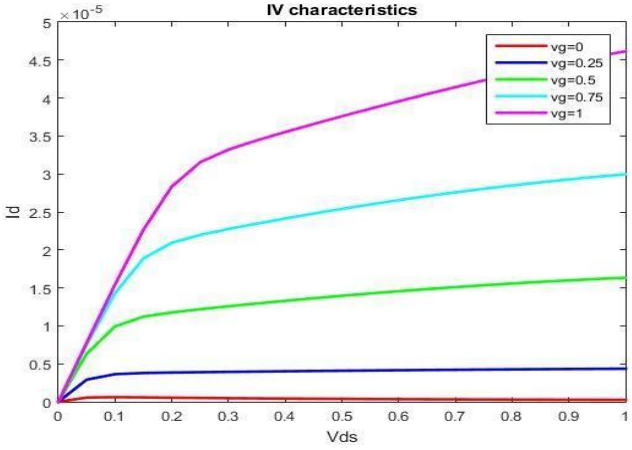

Figure 9: IV characteristics of Model 1

Proposed Drain Current Model

Drain current is a function of two independent variables, VGS and VDS. Plotting $IDS(VGS,VDS)$ in its most general case results in a three-dimensional surface. Modeling a molecular FET using a two-variable parametric polynomial requires numerous parameters, so the conventional MOSFET model is employed:

$$I_D = \begin{cases} \frac{\mu C_0 W}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}], & \text{for } V_{DS} < V_{DS,sat} \\ \frac{1}{2}\mu C_0 \frac{W}{L}(V_{GS} - V_{th})^2[1 + \lambda V_{DS}], & \text{for } V_{DS} \geq V_{DS,sat} \end{cases}$$

Where, variables VGS and VDS are used along with parameters μ,C0, W, and Vth . The polynomial approximations for the parameters A and B are;

$$A = a_0 + a_1 x + a_2 y + a_3 x^2 + a_4 xy + a_5 y^2$$

$$B = b_0 + b_1 x + b_2 y + b_3 x^2 + b_4 xy + b_5 y^2$$

Where,

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$a0=4.07*10^{-5}$,	$a1=11.99*10^{-5}$	$a2=11.10*10^{-5}$	$a3=-8.84*10^{-5}$	$a4=-5.65*10^{-5}$	$a5=1.56*10^{-5}$
$b0=1.5*10^{-5}$	$b1=2.58*10^{-5}$	$b2=12.75*10^{-5}$	$b3=1.39*10^{-5}$	$b4=5.80*10^{-5}$	$b_5=-0.916*10\text{^}-5$

Table 2: Average CPU calculation time for DFTB+, Model 1 and proposed model

	DFTB+	Model1	Proposed model
For 1 sweep	12537 seconds	0.035223 seconds	0.00073 seconds
For single value	597 seconds	0.001677 seconds	3.476e-6 seconds

Intel(R) Core (TM) i7-4770 CPU@ 3.40 GHz was used for analysis.

Table 3: Current calculation using DFTB+ analysis and proposed model current in Matlab.

Fermi level (S&D)	Vds	Energy range	ID for Vgs=0 μA		ID for Vgs=0.2 μA		ID for Vgs=0.4 μA		ID for Vgs=0.6 μA		ID for Vgs=0.8 μA	
			Dftb+	Proposed model	Dftb+	Proposed model	Dftb+	Proposed model	Dftb+	Proposed model	Dftb+	Proposed model
-4.7103	0.0	-6.5 to -3.0	5.2e-14	7.8e-12	6.78e-14	0	1.32e-14	0	0	0	1.36e-14	0
-4.7103	0.2	-6.5 to -3.0	0.000000726	2.23e-11	0.63	0.81	12.8	7.89	20.4	14.93	30.2	19.44
-4.7103	0.4	-6.5 to -3.0	0.000000951	2.23e-11	0.78	0.83	13.3	9.35	27.5	23.1	44.8	33.02
-4.7103	0.6	-6.5 to -3.0	0.00000125	4.3e-11	0.89	0.85	14.4	9.72	29.5	25.2	51.2	40.8
-4.7103	0.8	-6.5 to -3.0	0.00000163	7.3e-11	1.19	0.91	15.1	10.08	31.8	26.2	52.6	43.2
-4.7103	1	-6.5 to -3.0	0.00000214	1.05e-10	1.32	0.94	15.89	10.45	33.5	27.21	53.9	44.9

Intel(R) Core (TM) i7-4770 CPU@ 3.40 GHz was used for analysis. There is slight difference in current values of our proposed model as compared to dftb+ calculation, which validates equivalent model results.

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Comparison

The proposed CNTFET model is compared with the FETtoy model from NanoHub to evaluate its accuracy and performance. The I-V characteristics for different gate voltages (0-1V) are illustrated in Figure 5.3, showcasing variations in CNT diameter, drain control parameters, and threshold voltage. An increase in CNT diameter from 2nm to 3nm results in a reduction of the threshold voltage, as the band gap is inversely proportional to the diameter. This change also affects the ON current, as a larger CNT diameter leads to a smaller band gap, which in turn enhances current flow. Additionally, lowering the drain control parameter reduces the overall current, as this parameter influences drain-induced barrier lowering (DIBL), affecting device efficiency.

The transfer characteristics of the CNTFET model, depicting the relationship between drain current and gate voltage for different drain voltages, are presented in Figure 5.4. The results from the proposed model closely align with those obtained from the FETtoy model, demonstrating the model's reliability. However, a minor discrepancy is observed at lower drain voltages, where the proposed model shows slight saturation. This difference arises due to the capacitance, which is not analytically calculated in the proposed model but instead depends on the contact between the CNT channel and the source/drain.

Model Validation

To further validate the proposed model, it was implemented at the circuit level using VHDL-AMS and tested on digital circuits, including NAND gates, inverters, and phase detectors. For the NAND gate experiment, a CNTFET-based NAND gate was designed, and its circuit diagram is provided in Figure 5.5. The corresponding input/output waveforms, as shown in Figure

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demonstrate the expected behavior, with parasitic capacitance effects clearly visible in the output signal.

A CNTFET-based phase detector (PD) was also designed using the proposed model. This circuit operates as an open-loop phase detector, which detects phase differences by comparing a reference signal with an input signal. If both signals are in phase, the output remains at zero, whereas an out-of-phase condition results in an output signal of one. The circuit diagram of the phase detector is illustrated in Figure 5.7, while the corresponding waveform output is depicted in Figure 5.8. The results confirm that the phase detector operates within the expected range, further validating the model's accuracy. Additionally, the proposed model demonstrates lower power consumption and reduced propagation delay compared to conventional MOSFET-based circuits. These improvements suggest that CNTFET-based circuits respond more efficiently to input changes, making them a promising alternative for future nanoelectronics applications.

Conclusion

One of the most promising Nano devices is the carbon nanotube transistor. Ideal CNT transistor based logic circuits can provide significant energy and performance benefits over silicon CMOS. The purposes of this thesis were to study electronic properties of CNTs, to model I-V characteristics of MOSFET-like CNTFET and finally to validate the model by constructing circuits. The main objectives are achieved. First section was devoted to understand Basic electronic properties of CNTs, which were studied in order to create device. Energy band structure, density of state and carrier density were investigated.in second section OPV molecule was analyzed which served as a basis for CNTFET modelling. In third section fully analytical

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model of MOSFET-like CNTFET is developed. The model requires no iteration or numerical simulation and thus can be used for circuit- level simulation. The model developed is unique in that it is fully analytical model that considered induction of parameters and avoid time consuming calculations. Various parameters such as gate insulator thickness, gate insulator dielectric constant, diameter, channel length and temperature are varied to see the performance dependency. These parameters were approximated by polynomial curve fitting which avoids time and again calculation of effect of these parameters and hence it is considered a generic model. Developed model was tested by comparing its simulation results with that of experimentally reported results from NanoHub. The comparison results give a good agreement which shows the accuracy of the development model. In order to see the effect of scaling of physical parameters on the performance of CNTFET, we made simulations in DFTB+ software by varying these parameters, specifically by varying gate oxide thickness and drain control parameters. Reducing insulator thickness improves performance significantly. Increasing dielectric constant of gate insulator also improves performance. However, increasing dielectric constant will not always improve performance constantly. From simulations it is observed that voltage and diameter are inversely related. Results showed that On-state current increased with the increase in diameter of carbon nanotube. Similar to diameter scaling case, there was an increase in current. Finally, using our VHDL-AMS model we constructed circuits such as NAND gate, inverter and phased detector and analyzed them.

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